IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
BEAUMONT DIVISION

DR. URI COHEN	§	
	§	
Plaintiff,	§	
	§	
v.	§	Case No. 1:17-CV-189
	§	
TSMC NORTH AMERICA CORP., TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD., HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HISILICON TECHNOLOGIES CO., LTD., AND APPLE, INC.	§	Jury Demanded
	§	
Defendants.	§	

PLAINTIFF'S ORIGINAL COMPLAINT

Dr. Uri Cohen brings this action against Taiwan Semiconductor Manufacturing Company, Ltd., TSMC North America Corp. (collectively, "TSMC"), Huawei Technologies Co., Ltd., Huawei Device USA Inc., Futurewei Technologies, Inc., HiSilicon Technologies Co., Ltd. (collectively, "Huawei"), and Apple, Inc. ("Apple"), and alleges as follows:[1]

THE PARTIES

1. Plaintiff Dr. Uri Cohen ("Plaintiff" or "Dr. Cohen") is a United States citizen, with a residence of 4147 Dake Ave., Palo Alto, CA 94306.

2. Defendant Taiwan Semiconductor Manufacturing Company Ltd. is a Taiwanese corporation and is headquartered at No. 8, Li-Hsin Rd. VI, Hsinchu, Taiwan 300, R.O.C., and has as its wholly owned U.S. subsidiary Defendant TSMC North America Corp., headquartered at

[1] Except where otherwise noted or apparent from context, any allegation against "Defendants," "TSMC," or "Huawei," is an allegation directed to every defendant subsumed within that name.

2585 Junction Avenue, San Jose, California 95134 (collectively, "TSMC"). TSMC North America Corp. may be served through its registered agent Steven A. Schulman, located at 2585 Junction Ave., San Jose, California 95134.

3. Defendant Huawei Technologies Co., Ltd. ("Huawei China") is a corporation organized and existing under the laws of China, with its principal place of business at Bantian, Longgang District, Shenzhen 518129, P.R. China. Upon information and belief, Defendant Huawei China is authorized to do business in Texas and has a North American Headquarters for Marketing, Sales & Services located at 5700 Tennyson Parkway, Suite 500, Plano, Texas 75024.

4. Defendant Huawei Device USA Inc. ("Huawei USA") is a Texas corporation with its principal place of business in Plano, Texas. Huawei USA distributes, markets, and sells mobile devices, including smartphones in the United States. Upon information and belief, Defendant Huawei USA is authorized to do business in Texas and has a North American Headquarters for Marketing, Sales & Services located at 5700 Tennyson Parkway, Suite 500, Plano, Texas 75024. Huawei USA may be served through its registered agent CT Corporation System, 350 N. St. Paul Street, Suite 2900, Dallas, Texas 75201.

5. Defendant HiSilicon Technologies Co., Ltd. ("HiSilicon") is a Chinese company with its principal place of business in Bantian, Longgang District, Shenzhen, People's Republic of China. On information and belief, HiSilicon is a subsidiary of Huawei China, and has a design division in Silicon Valley, U.S.A.

6. Defendant Futurewei Technologies, Inc., ("Futurewei") is an indirect subsidiary of Huawei China, and is a corporation organized and existing under the laws of Texas, with its principal place of business at 5700 Tennyson Parkway, Suite 500, Plano, Texas 75024.

7. Defendant Apple Inc. ("Apple") is a California corporation with a principal place of business at 1 Infinite Loop, Cupertino, California 95014. Apple has designated CT Corporation System, 350 N. St. Paul Street, Suite 2900, Dallas, Texas 75201 as its agent for service of process.

JURISDICTION AND VENUE

8. This action arises under the patent laws of the United States, Title 35 United States Code, particularly §§ 271 and 281. This Court has jurisdiction over these claims for patent infringement under 28 U.S.C. §§ 1331 and 1338(a).

9. Personal jurisdiction exists generally over TSMC, Huawei China, Huawei USA, HiSilicon, Futurewei, and Apple because those companies have sufficient minimum contacts with the forum as a result of business conducted within the State of Texas and within the Eastern District of Texas. For example, Huawei China's United States headquarters and Huawei USA's and Futurewei's main headquarters are all located in this district; Apple has a major office in this state, and retail sales locations throughout the state and this District; and on information and belief TSMC has significant contacts with its customers and fellow market participants in the state and this District, including Huawei and Apple. Personal jurisdiction also exists specifically over TSMC, Huawei, and Apple because those companies, directly or through subsidiaries or intermediaries, make, use, offer for sale, or sell products or services within the State of Texas and within the Eastern District of Texas that directly or indirectly infringe the patents-in-suit.

10. Venue is proper in this Court under Title 28 United States Code §§ 1391(b) and (c) and 1400(b) at least because TSMC, Huawei, and Apple are subject to personal jurisdiction in this district and have regularly conducted business in this district, and because certain of the acts complained of herein occurred in this district.

THE PATENTS

11. On February 11, 2003, U.S. Patent No. 6,518,668 entitled "Multiple Seed Layers for Metallic Interconnects" ("the '668 patent") was duly and legally issued. A true and correct copy of the '668 patent is attached as Exhibit 1.

12. Pursuant to 35 U.S.C. § 282, the '668 patent is presumed valid.

13. Dr. Cohen is the owner of the entire right, title, and interest in the '668 patent, including the right to sue and collect damages for past, present, and future infringement (to the extent those remedies are available to him).

14. On August 2, 2005, U.S. Patent No. 6,924,226 entitled "Methods for Making Multiple Seed Layers for Metallic Interconnects" ("the '226 patent") was duly and legally issued. A true and correct copy of the '226 patent is attached as Exhibit 2.

15. Pursuant to 35 U.S.C. § 282, the '226 patent is presumed valid.

16. Dr. Cohen is the owner of the entire right, title, and interest in the '226 patent, including the right to sue and collect damages for past, present, and future infringement (to the extent those remedies are available to him).

17. On April 3, 2007, U.S. Patent No. 7,199,052 entitled "Seed Layers for Metallic Interconnects" ("the '052 patent,") was duly and legally issued. A true and correct copy of the '052 patent is attached as Exhibit 3.

18. Pursuant to 35 U.S.C. § 282, the '052 patent is presumed valid.

19. Dr. Cohen is the owner of the entire right, title, and interest in the '052 patent, including the right to sue and collect damages for past, present, and future infringement (to the extent those remedies are available to him).

20. On October 16, 2007, U.S. Patent No. 7,282,445 entitled "Multiple Seed Layers for Interconnects" ("the '445 patent,") was duly and legally issued. A true and correct copy of the '445 patent is attached as Exhibit 4.

21. Pursuant to 35 U.S.C. § 282, the '445 patent is presumed valid.

22. Dr. Cohen is the owner of the entire right, title, and interest in the '445 patent, including the right to sue and collect damages for past, present, and future infringement (to the extent those remedies are available to him).

23. The '668 patent, '226 patent, '052 patent, and '445 patent will hereinafter be referred to collectively as the "patents-in-suit."

24. To the extent required, Dr. Cohen has complied with the marking provisions of 35 U.S.C. § 287 and is thus entitled to past damages.

DR. COHEN'S PRIOR COMMUNICATIONS WITH TSMC

25. Dr. Cohen was first introduced to TSMC in October 2000. After getting in touch with Mr. Henry Lo of TSMC in Taiwan, Dr. Cohen was invited by TSMC to present his Seed Layers technologies to TSMC in Hsinchu, Taiwan. Dr. Cohen provided TSMC a presentation of his technologies on April 10, 2001. Among other things, Dr. Cohen explained to TSMC how it could use a chemical vapor deposition ("CVD") seed layer followed by a physical vapor deposition ("PVD") seed layer over a barrier layer to enable reliable void-free electrofill of openings narrower than 0.10 micron for TSMC's current and future generations of interconnects.

26. After the meeting in Hsinchu in April 2001, Dr. Cohen followed up a number of times with TSMC in subsequent months. Ultimately, TSMC declined at that time to collaborate with Dr. Cohen, or take a license to Dr. Cohen's patent-pending technologies.

27. In 2003, Dr. Cohen reached out again to TSMC, getting in touch with Dr. Rick Tsai, the president of TSMC at that time. Dr. Cohen had several communications with Dr. Tsai in which Dr. Cohen suggested to TSMC that it take a license to what Dr. Cohen referred to as his "Seed Layer Portfolio," and indicated that several patents had issued, including U.S. Patent No. 6,518,668 and a Taiwanese counterpart. Dr. Cohen explained to TSMC, among other things and as he had done before, that as geometries of semiconductor chips become smaller, Dr. Cohen's patented technology would become more relevant to TSMC's chip designs and methods of fabrication. Once again, TSMC declined to take a license to Dr. Cohen's patents.

28. On July 23, 2004, Dr. Cohen (through his counsel) sent a letter to Dr. Richard Thurston, TSMC's then-Vice President and General Counsel, drawing TSMC's attention once again to the '668 patent, among others, and providing TSMC a copy of the '668 patent. Included with that letter, Dr. Cohen provided TSMC a general description of the patented technology and patents pending in Dr. Cohen's Seed Layer Portfolio.

29. Dr. Cohen also provided TSMC with claim charts explaining the manner in which certain of Dr. Cohen's claims would be infringed by specific forms of interconnects, including representative claim charts for the '668 patent. Having received no reply from Dr. Thurston, on October 12, 2004 Dr. Cohen sent another letter to Dr. Thurston, in which he strongly recommended that TSMC consider taking a license to Dr. Cohen's patents. He urged that even if TSMC did not yet use Dr. Cohen's patented technology, it soon likely would as its technology nodes moved to smaller geometries.

30. Thereafter, from 2004 through 2007, Dr. Cohen's counsel communicated with TSMC on numerous occasions concerning Dr. Cohen's patented technology.

31. For example, on May 1, 2006, Dr. Cohen's counsel sent a letter to Steven Slater, Esq., TSMC's outside counsel with the law firm Slater & Matsil, LLP, drawing TSMC's attention to the '226 patent, among others, and providing TSMC a copy of the '226 patent and explaining how TSMC would infringe the '226 patent if it employed certain processing methods.

32. That letter also identified to TSMC Dr. Cohen's U.S. Application No. 2007-0117379, which subsequently matured into the '052 patent.

33. TSMC denied again that it was infringing any of Dr. Cohen's patents, and in a letter dated October 6, 2006, explained:

> We would like to leave the door open to licensing Dr. Cohen's patents in the future, should TSMC elect to adopt multiple layer seed processes that are relevant to Dr. Cohen's patent claims, but TSMC is not using such technology at the present time and has no current plans to do so.

34. In a letter dated June 29, 2007, Dr. Cohen's counsel directed TSMC's attention to, among others, claims 10, 17, 18, 26, 33, 34, 53, and 58, of the '052 patent.

35. As further evidence that TSMC has been well aware of Dr. Cohen's patented technology, TSMC has referenced Dr. Cohen's '668 patent in no less than 15 of its own patents and patent applications, including U.S. Patent Nos. 6806192, 6943111, 7067409, 7215024, 7265038, 7378744, 8277619, and U.S. Patent Applications Nos. 20040147104, 20040157431, 20050029665, 20050110147, 20050250320, 20050263902, 20060216916, and 20070010080.

BACKGROUND FACTS CONCERNING ACCUSED PRODUCTS

36. All preceding paragraphs are incorporated by reference as if fully set forth herein.

37. An integrated circuit is a set of electronic circuits integrated on semiconductor material, which is most often silicon. These are often referred to as "semiconductor devices" or "semiconductor chips." These semiconductor chips are used in electronics, computers, and smartphones, among other devices.

38. TSMC fabricates integrated circuits for a number of companies using its 20 and 16 nanometer node finFET process.

39. For example, TSMC fabricates the HiSilicon Kirin 950 and 955 chips (16nm) for Huawei for use in at least the Huawei P9 and Huawei Honor 8 Smartphones (the "Huawei Chips").

40. TSMC also fabricates the Apple A8 (20nm), Apple A9 (16nm), and Apple A10 (16nm) Applications Processors (and their variants, including the A8X and the A9X) for Apple (the "Apple Chips").[2]

41. TSMC similarly fabricates modems, CPUs, GPUs, FPGAs, and other chips for numerous other companies using its 16 and 20 nanometer finFET process (the "Other 16nm and 20nm Chips").

42. Though TSMC does not publicly disclose all of its customers for its 16nm and 20nm node processes, on information and belief the Other 16nm and 20nm Chips are functionally identical to the Huawei Chips and the Apple Chips for purposes of this Complaint, are fabricated by TSMC using the same fabrication method, and have the same relevant structures.

43. For example, Dr. Cohen's reverse engineering analysis of the Apple Chips and the Huawei Chips (discussed further below) has revealed that those chips, fabricated at the same or similar nodes, contain the same relevant structures for purposes of this Complaint (including at least the metal layers).

44. Dr. Cohen's reverse engineering analysis of additional chips manufactured using TSMC's 16nm or 20nm nodes has revealed that those chips too contain the same relevant structures for purposes of this Complaint.

[2] The Apple Chips are incorporated into the Apple iPhone 6 and iPhone 7 generation smart phones and tablets.

45. TSMC's 16 nanometer node interconnect technology is in all relevant ways identical to its 20 nanometer node interconnect technology, as they both share the same metal backend process.[3]

46. On information and belief, it is industry practice that when a large chip fabricator like TSMC adopts a certain process for a specific node (such as a process for applying seed layers for metallic interconnects), it uses that same process for all chips fabricated at that same node.

47. Therefore, on information and belief, all Other 16nm and 20nm Node Chips have identical relevant structures for purposes of this Complaint.

48. Hereinafter, the Huawei Chips, Apple Chips, and Other 16nm and 20nm Chips will be referred to collectively as the "Accused Chips."

49. The Accused Chips comprise integrated circuits that comprise multiple-seed-layer structures.

50. HiSilicon designs, develops, and supplies the Huawei Chips for incorporation into Huawei's mobile devices. Huawei incorporates the Huawei Chips it receives from HiSilicon into at least the Huawei P9 and Huawei Honor 8 Smartphones. HiSilicon works closely with TSMC on the design of the Huawei Chips:

> **TSMC 16FF+ Manufactured**
>
> As mentioned earlier, the Kirin 950 is HiSilicon's first TSMC 16FF+ manufactured mobile SoC. This also makes the Chinese vendor second in line after Apple's to release mobile silicon based on the new manufacturing node.
>
> HiSilicon explains that along with Apple they've been the two main lead partners of [TSMC], and both parties have been working closely together to try to improve the

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[3] http://www.tsmc.com/english/dedicatedFoundry/technology/16nm.htm; *see also* http://www.dailytech.com/TSMC+Hypes+Its+Upcoming+10+nm+Process+Amid+Struggles+to+Hit+Volume+at+16+nm/article37298.htm ("TSMC's strategy to achieve 16 nm production is controversial, as it's built 'on top of' TSMC's 20 nm process. It uses 16 nm transistors. However, for the backplane it uses 20 nm interconnects (bonding pads, electrical contacts, insulating layers, and metal layers).").

> design and to tune the process. In fact, the company revealed that first mass production (also commonly named as risk production) started as early as last January. Over the following months both companies cooperated to sort out bugs and imperfections in the design (chip revisions) to go up from 20% yield in the earliest runs to up to 80% yields and qualified mass production this last August.[4]

51. Apple designed the Apple Chips which are made by TSMC for Apple. With respect to the design of its A8, Apple has explained:

> iPod touch features an Apple-designed A8 chip built on 64-bit architecture. This desktop-class chip features GPU performance up to 10 times faster than the previous-generation iPod touch — so the graphics in your favorite games are more responsive and look more vivid than ever before — and CPU performance is up to six times faster. And you get the same great battery life, with up to 40 hours of music and 8 hours of video playback.[5]
>
> The all-new A8 chip is our fastest yet. Its CPU and graphics performance are faster than on the A7 chip, even while powering a larger display and incredible new features. And because it's designed to be so power efficient, the A8 chip can sustain higher performance. . . . A8 uses an advanced 20-nanometer process. It's a remarkably small and efficient chip on which two billion transistors deliver incredible performance with up to 50 percent more energy efficiency than the A7 chip.[6]

52. With respect to the design of its A9 chips, Apple has explained:

> The A9 chip brings a new level of performance and efficiency to iPhone 6s. Not only a faster experience, but a better one. The A9 chip is capable of gaming console–class graphics performance that makes games and other apps much richer and more immersive.
>
> . . . The A9 chip is our third-generation chip with 64-bit architecture. It sits at the cutting edge of mobile chips, improving overall CPU performance by up to 70 percent compared to the previous generation. And boosting graphics performance by up to a staggering 90 percent compared to the previous generation.[7]

53. TSMC uses its 16 nanometer node finFET process to fabricate the A9 and A10 processors.[8,9]

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[4] http://consumer.huawei.com/en/press/media-coverage/hw-462408.htm
[5] http://www.apple.com/ipod-touch/
[6] http://www.apple.com/iphone-6/technology/
[7] http://www.apple.com/iphone-6s/technology/
[8] http://www2.techinsights.com/l/8892/2015-09-28/zxx9c;
[9] http://appleinsider.com/articles/16/07/11/apple-chip-builder-tsmc-expected-to-see-record-q3-on-a10-chips; https://en.wikipedia.org/wiki/Apple_A10; http://appleinsider.com/articles/16/06/30/tsmc-expected-to-net-big-revenue-boost-on-apple-a10-chips-for-iphone-7

54. With respect to the design of its A10 chips, Apple has explained:

> iPhone 7 is supercharged by the most powerful chip ever in a smartphone. It's not just faster than any previous iPhone — it's also more efficient. That's because the A10 Fusion chip uses an all-new architecture that enables faster processing when you need it, and the ability to use even less power when you don't. And with the longest battery life ever in an iPhone, you can work at twice the speed of iPhone 6 and still enjoy more time between charges.
>
> With an all-new four-core design, the A10 Fusion chip's CPU has two high-performance cores and two high-efficiency cores. The high-performance cores can run at up to 2x the speed of iPhone 6, while the high-efficiency cores are capable of running at just one-fifth the power of the high-performance cores. That means you get the best performance and efficiency when you need it.[10]

55. Based in part on the allegations in paragraphs 49-53, above, as well as on other reports of collaboration between TSMC and its customers, on information and belief TSMC also cooperates with its customers for the Other 16nm and 20nm Chips, including by collaborating on chip design, coauthoring papers and articles, etc.

56. In 2010, in an article titled "A New Enhancement Layer to Improve Copper Interconnect Performance," and published in the IEEE International Technology Conference, TSMC reported that the use of cobalt as a seed/enhancement layer between a PVD tantalum barrier layer and a copper seed layer would improve copper wetting on the barrier layer, improve interconnect quality, electrical performance, reliability, and maximize gap fill in integrated circuits ("TSMC's IEEE Paper").[11]

57. To achieve this integrated circuit design in its 20 nanometer and 16 nanometer node technologies, as reported in TSMC's IEEE Paper, TSMC on information and belief utilizes

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[10] https://www.apple.com/iphone-7/

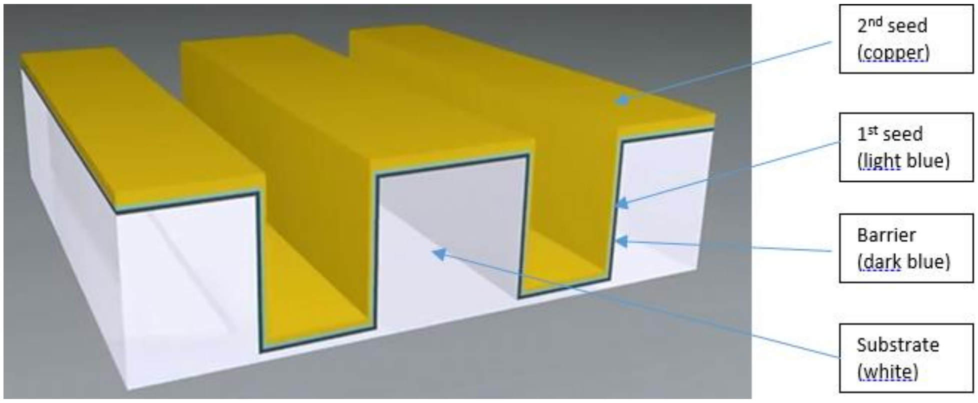
[11] http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=5510762&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D5510762

equipment supplied to it by Applied Materials, Inc. ("AMAT"), including AMAT's Endura platform and Endura Volta System.

58. The Endura platform supports both Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD) processes,[12] including the Endura Volta System, which was introduced by AMAT on May 13, 2014.[13]

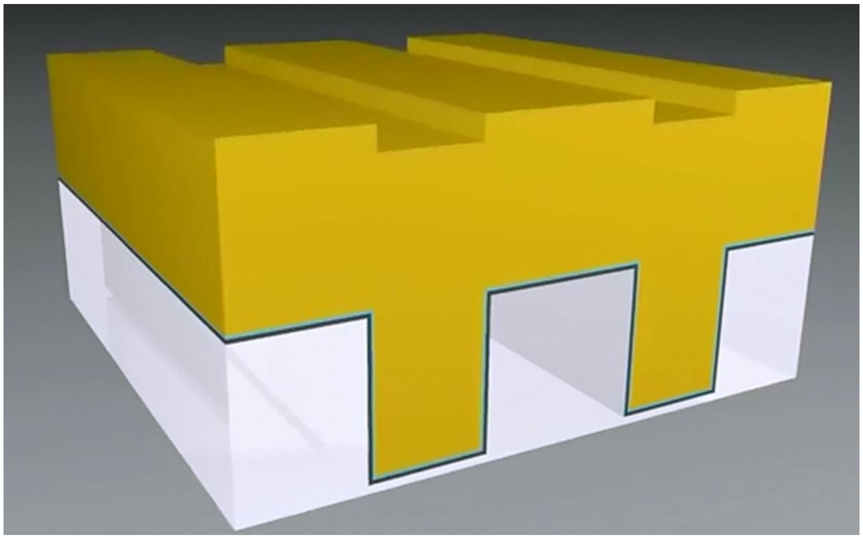
59. On information and belief, the method utilized by TSMC to manufacture the Accused Chips and the resulting structure of the Accused Chips themselves are consistent with the methods and structures as explained by TSMC in its IEEE Paper, and as depicted below.

60. As shown here, the resulting 20 nanometer and 16 nanometer devices fabricated by TSMC contain a multiple seed layer structure comprising a patterned insulating layer formed on a substrate, a tantalum barrier layer over the substrate, a first seed layer comprising cobalt, a second seed layer comprising copper, and an electroplated metallic layer of copper disposed over the second seed layer:[14]

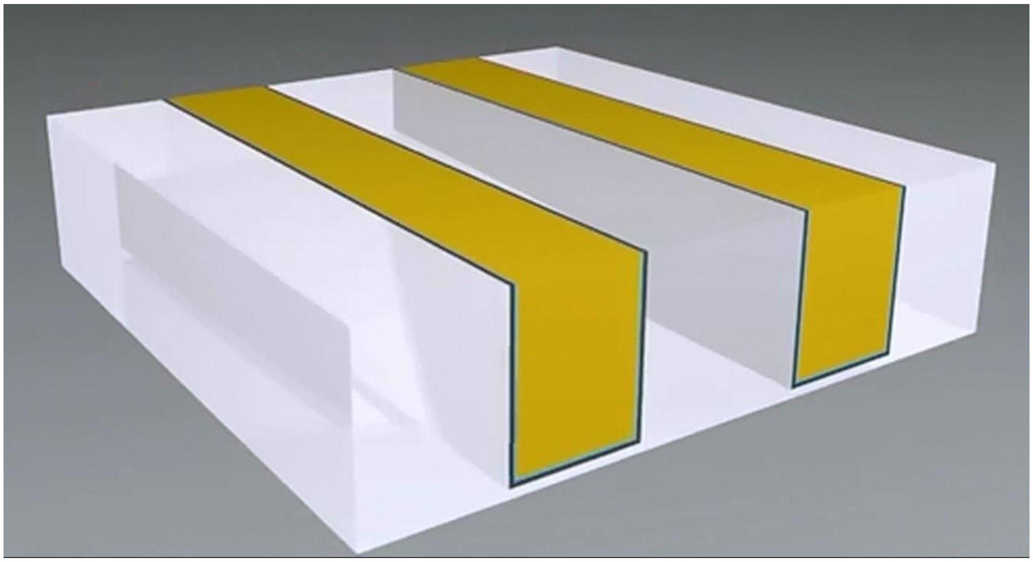


[12] *Id.*
[13] http://www.appliedmaterials.com/company/news/press-releases/2014/05/applied-materials-introduces-the-biggest-materials-change-to-interconnect-technology-in-15-years
[14] *See* "Volta Animation," appliedschannel, https://www.youtube.com/watch?v=EcWdzKRK2dk.

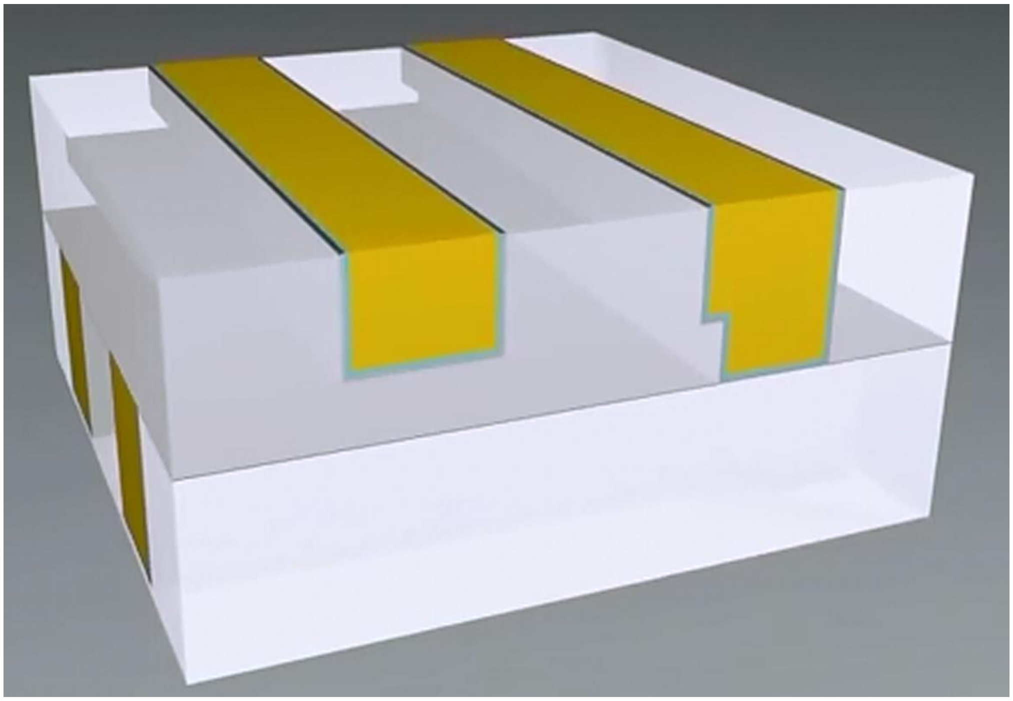
61. After the barrier, first seed layer and second seed layer are formed over the substrate, electroplated copper is disposed over the second seed layer over the openings and the field, as depicted below.



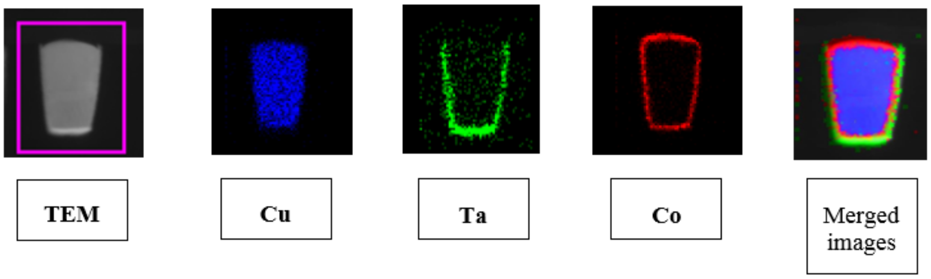
62. After the electroplated copper is disposed over the openings and the field, the electroplated copper overlying the field, the first and second seed layers overlying the field, and the barrier layer overlying the field are all substantially removed by a polishing technique. The resulting interconnect is as is depicted below.



63. Multiple levels of interconnects are often stacked one on top of another, which is the case with the Accused Chips, as depicted below.



64. Confirming the existence of the structure depicted above in the Accused Chips, the images below depict actual cross-sections of interconnects in the Apple Chips and Huawei Chips obtained via reverse engineering.



65. The presence of a cobalt ("Co") seed layer in these cross-sections confirms the use in the Accused Chips of the multiple-seed-layer process described above.

66. The images are unable to depict a distinct copper seed layer on top of the cobalt seed layer because electroplating merges the copper seed layer with the electroplated copper, as illustrated in paragraphs 59-60 and 63, above.

67. However, on information and belief, achieving the copper metallization depicted in the cross-section images is accomplished by first applying a copper seed layer on top of the cobalt seed layer prior to electroplating, as illustrated in paragraphs 59 and 60.

BACKGROUND INFORMATION CONCERNING DEFENDANTS' ACTS OF INFRINGEMENT

68. All preceding paragraphs are incorporated by reference as if fully set forth herein.

69. The Accused Chips meet or embody the limitations of the at least one claim of each of the patents-in-suit, as described further below in Counts I–IV.

70. The Defendants have infringed at least one claim of each of the patents-in-suit by making, using, selling, offering for sale within the United States and/or importing into the United States, the Accused Chips; or induced infringement of the same.

71. More specifically, on information and belief, Defendant TSMC makes the Huawei Chips for Huawei, then offers to sell and sells the Huawei Chips for use in the United States.

72. Huawei imports, offers to sell, and/or sells devices containing the Huawei Chips (such as the Huawei P9 and Huawei Honor 8 Smartphones) in the United States.

73. On information and belief, Defendant TSMC makes the Apple Chips for Apple, then offers to sell and sells the Apple Chips for use in the United States.

74. Apple imports, offers to sell, and sells devices containing the Apple Chips (such as the Apple iPhone 6 and iPhone 6 Plus, iPhone 6S and iPhone 6S Plus, iPhone SE, iPad Touch, iPad Pro (12.9"), iPad Pro Mini (9.7"), iPhone 7 and iPhone 7 Plus) in the United States.

75. On information and belief, Defendant TSMC makes the Other 16nm and 20nm Chips for its other customers, then offers to sell and sells the Other 16nm and 20nm Chips for use in the United States.

76. TSMC's customers and their affiliates—including but not limited to Apple, Huawei, other equipment manufacturers, chip designers, and chipset makers—import, offer to sell, and/or sell devices containing the Other 16nm and 20nm Chips (including the Apple devices listed above, the Huawei devices listed above, and Huawei's Google Nexus 6P) in the United States.

77. On information and belief, Huawei uses devices containing the Accused Chips in the United States, during testing, demonstrations, and the like.

78. On information and belief, Apple uses devices containing the Accused Chips in the United States, during testing, demonstrations, and the like.

A. DEFENDANTS' DIRECT INFRINGEMENT

1. TSMC'S Direct Infringement

79. All preceding paragraphs are incorporated by reference as if fully set forth herein.

80. TSMC directly infringes at least one claim of each of the patents-in-suit, either literally or under the doctrine of equivalents, by selling and/or offering for sale within the United States the Accused Chips.

81. On information and belief, TSMC collaborates with its customers in the United States regarding the design of the Accused Chips.

82. On information and belief, TSMC conducts marketing efforts related to the Accused Chips in the United States.

83. On information and belief, TSMC engages in pricing and contractual negotiations regarding the Accused Chips with customers in the United States.

84. On information and belief, TSMC receives purchase orders for Accused Chips in the United States.

85. On information and belief, TSMC executes contracts for sale of the Accused Chips in the United States.

86. Many of the Accused Chips are ultimately sold, offered for sale, and used in devices within the United States.

87. On information and belief, TSMC knows that many of the Accused Chips it sells its customers will ultimately be sold, offered for sale, and used in devices within the United States.

2. Huawei's Direct Infringement

88. All preceding paragraphs are incorporated by reference as if fully set forth herein.

89. Huawei directly infringes at least at least one claim of each of the patents-in-suit under 35 U.S.C. 271(a) and 271(g), either literally or under the doctrine of equivalents, by making, using, selling, offering for sale within the United States, leasing, and/or importing into the United States, devices that incorporate the Accused Chips (including at least the Huawei P9, Huawei Honor 8, and Google Nexus 6P Smartphones).

90. The Accused Chips made by the processes claimed in the asserted process claims of the patents-in-suit are not materially changed by subsequent processes prior to importation, use, sale, or offer for sale in the United States by Huawei.

91. As demonstrated by the cross-section images and other information above, Dr. Cohen's patented multiple-seed-layer structure, and benefits thereof, remain discernible and intact in the Accused Chips as sold.

92. The Accused Chips made by the processes claimed in the asserted process claims of the patents-in-suit do not become a trivial or nonessential component of another product prior to importation, use, sale, or offer for sale in the United States by Huawei.

93. As demonstrated by the cross-section images and other information above, Dr. Cohen's patented multiple-seed-layer structure, and benefits thereof, remain discernible and intact in the Accused Chips as sold.

94. The Accused Chips, which include central processing units, graphics processing units, modems, etc., are essential to the operation of the electronic devices, chipsets, and other products the Accused Chips are incorporated into.

3. Apple's Direct Infringement

95. All preceding paragraphs are incorporated by reference as if fully set forth herein.

96. Apple directly infringes at least one claim of each of the patents-in-suit under 35 U.S.C. 271(a) and 271(g), either literally or under the doctrine of equivalents, by making, using, selling, offering for sale within the United States, leasing, and/or importing into the United States, smart phones and other devices that incorporate the Accused Chips (including at least the Apple iPhone 6 and iPhone 6 Plus, iPhone 6S, 6S Plus, iPhone SE, iPad Touch, iPad Pro (12.9"), iPad Pro Mini (9.7"), iPhone 7 and iPhone 7 Plus).

97. The Accused Chips made by the processes claimed in the asserted process claims of the patents-in-suit are not materially changed by subsequent processes prior to importation, use, sale, or offer for sale in the United States by Apple.

98. As demonstrated by the cross-section images and other information above, Dr. Cohen's patented multiple-seed-layer structure, and benefits thereof, remain discernible and intact in the Accused Chips as sold.

99. The Accused Chips made by the processes claimed in the asserted process claims of the patents-in-suit do not become a trivial or nonessential component of another product prior to importation, use, sale, or offer for sale in the United States by Apple.

100. As demonstrated by the cross-section images and other information above, Dr. Cohen's patented multiple-seed-layer structure, and benefits thereof, remain discernible and intact in the Accused Chips as sold.

101. The Accused Chips, which include central processing units, graphics processing units, modems, etc., are essential to the operation of the electronic devices, chipsets, and other products the Accused Chips are incorporated into.

B. DEFENDANTS' INDUCEMENT OF INFRINGEMENT

1. TSMC's Inducement of Infringement

102. All preceding paragraphs are incorporated by reference as if fully set forth herein.

103. TSMC has had actual knowledge of the '668 patent since as early as July 23, 2004, including representative claim charts and infringement analyses for the '668 patent.

104. Moreover, TSMC has referenced Dr. Cohen's '668 patent in no less than 15 patents and patent applications assigned to TSMC, including U.S. Patent Nos. 6,806,192, 6,943,111, 7,067,409, 7,215,024, 7,265,038, 7,378,744, 8,277,619, and U.S. Patent Applications Nos. 20040147104, 20040157431, 20050029665, 20050110147, 20050250320, 20050263902, 20060216916, and 20070010080. Additionally, TSMC has had actual knowledge of the '226 patent since as early as May 1, 2006, including representative claim charts and infringement analyses for the '226 patent.

105. Additionally, TSMC has had actual knowledge of the application that matured into the '052 patent (U.S. Application No. 2007-0117379) since as early as May 1, 2006, and then the '052 patent itself since as early as June 29, 2007.

106. Moreover, TSMC has referenced Dr. Cohen's '052 patent in at least two patents assigned to TSMC, including U.S. Patent Nos. 7,704,886 and 8,252,690.

107. Additionally, TSMC has had actual knowledge of the application that matured into the ’445 patent (that is, U.S. Application No. 11/654,478) since as early as June 29, 2007.

108. Upon information and belief, TSMC knew of, or was willfully blind towards, its infringement of the patents-in-suit at least since it began fabricating Huawei Chips, Apple Chips and Other 16nm and 20nm Chips.

109. Since becoming aware of, or being willfully blind towards, its infringement of the patents-in-suit, TSMC has continued to intentionally, actively, and knowingly make, use, sell, offer to sell, and/or import one or more of the Accused Chips through its retailers, resellers, and distributors, as well as in other ways.

110. Since becoming aware of the patents-in-suit, TSMC’s advertising, sales, and/or technical materials in relation to the Accused Chips have intentionally, actively, knowingly, and willfully contained and continue to contain instructions, directions, suggestions, and/or invitations that intentionally, actively, and knowingly invite, entice, lead on, influence, encourage, prevail on, move by persuasion, and/or cause the public, TSMC’s distributors, retailers, and customers (including the related Huawei entities and Apple) to thereby directly infringe (via § 271(a) and/or § 271(g)) at least one claim of each of the patents-in-suit, either literally or under the doctrine of equivalents.

111. TSMC has collaborated with its customers, including Apple and Huawei, on the design of the Accused Chips. Since becoming aware of, or being willfully blind towards, its infringement of the patents-in-suit, TSMC was willfully blind or knew that the public’s, the distributors’, the retailers’, and/or the customers’ using, importing, selling, and/or offering to sell the Accused Chips directly infringe (via § 271(a) and/or § 271(g)), either literally or under the doctrine of equivalents, at least one claim of each of the patents-in-suit.

112. For at least these reasons, as well as others that may be revealed through discovery, TSMC is liable for inducing infringement (via § 271(a) and/or § 271(g)) of the patents-in-suit, either literally or under the doctrine of equivalents.

COUNT I: INFRINGEMENT OF THE ’668 PATENT

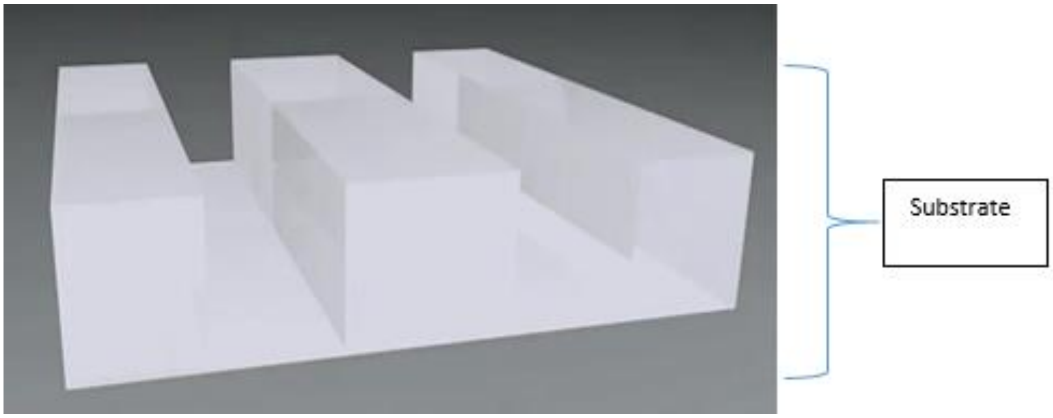
113. All preceding paragraphs are incorporated by reference as if fully set forth herein.

114. The Defendants have infringed at least one claim of the ’668 patent by performing the acts of infringement described above with respect to the Accused Chips.

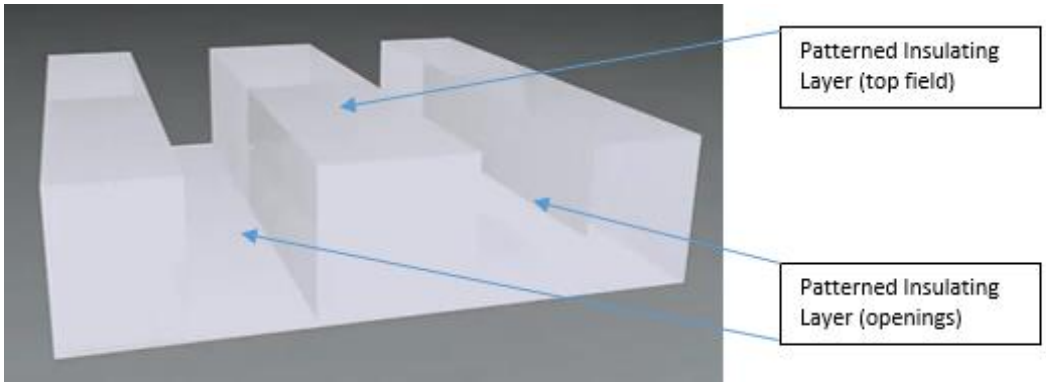
115. Each of the Accused Chips is fabricated by TSMC using the same relevant fabrication method, and producing the same relevant chip structure, as explained in the Volta Animation, and as described in paragraphs 49-53 and 58-66 above. As such, the Accused Chips meet each limitation of at least one claim of the ’668 patent.

116. By way of example and not limitation, each of the Accused Chips meets or embodies every limitation of claim 26 (dependent of claim 1) of the ’668 patent:

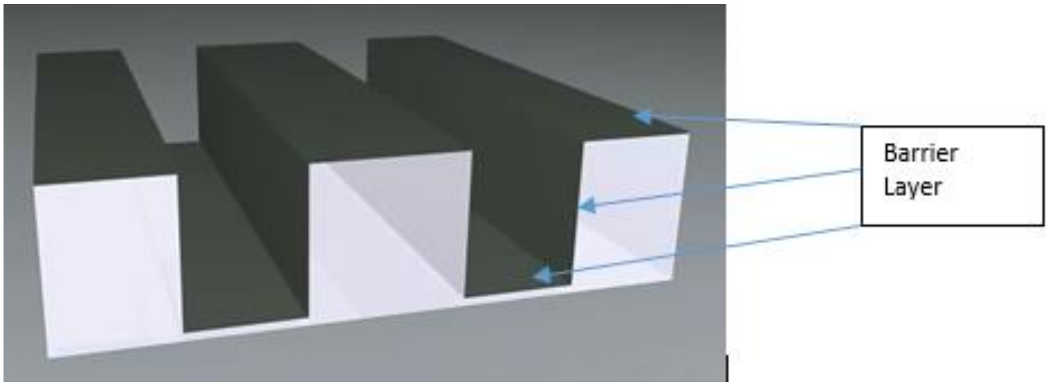
a. a substrate, as depicted below:



b. a patterned insulating layer formed on said substrate, said patterned insulating layer including at least one opening and a top field surface surrounding said at least one opening, as depicted below:

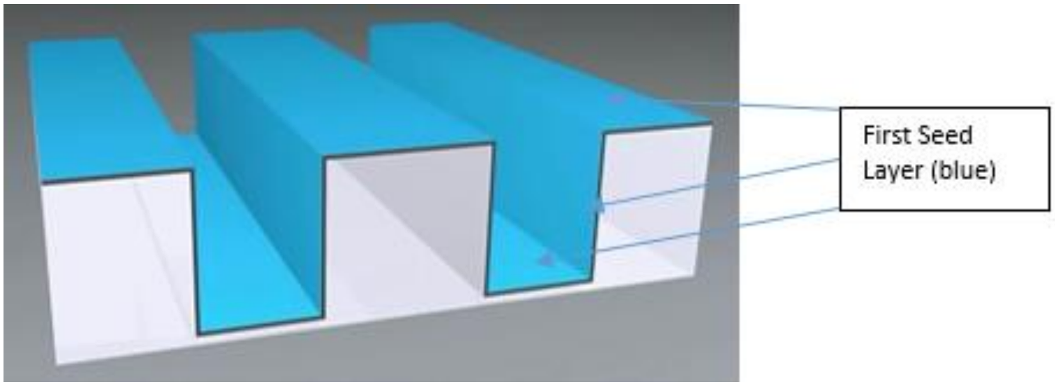

Patterned Insulating Layer (top field)
Patterned Insulating Layer (openings)

c. a barrier layer disposed over said patterned insulating layer including over inside surfaces of the at least one opening, as depicted below:


Barrier Layer

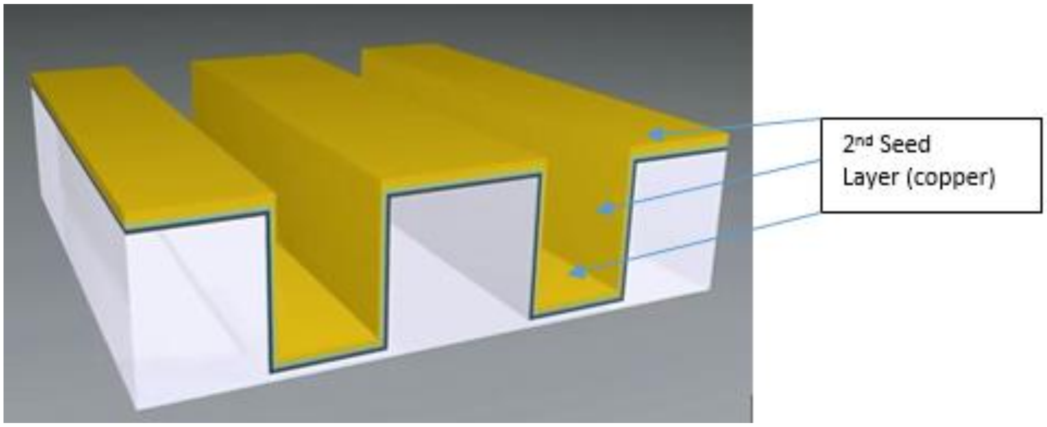
In the case of the Accused Chips, tantalum nitrite is used for the barrier layer and is applied through a PVD process.

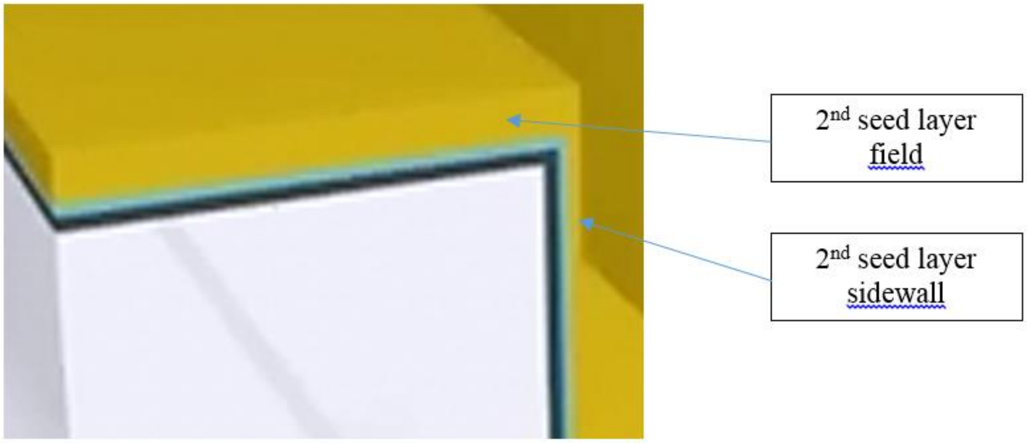
d. a first seed layer disposed over the barrier layer, said first seed layer comprising a substantially conformal seed layer whose thickness on the sidewalls of the opening (at about mid-depth) is about 25-100% of its thickness on the field, as depicted below:


First Seed Layer (blue)

A first conformal layer of cobalt is applied over the barrier layer through a CVD process. Because it is a conformal layer and applied through a CVD process, the thickness of the cobalt layer on the sidewalls of the opening (at about mid-depth) is about 25-100% of its thickness on the field.[15]

> e. a second seed layer disposed over the first seed layer, said second seed layer comprising a substantially non-conformal seed layer whose thickness on the sidewalls of the opening (at about mid-depth) is less than about 25% of its thickness on the field, and wherein said second seed layer being thicker than said first seed layer over the field, as depicted below:

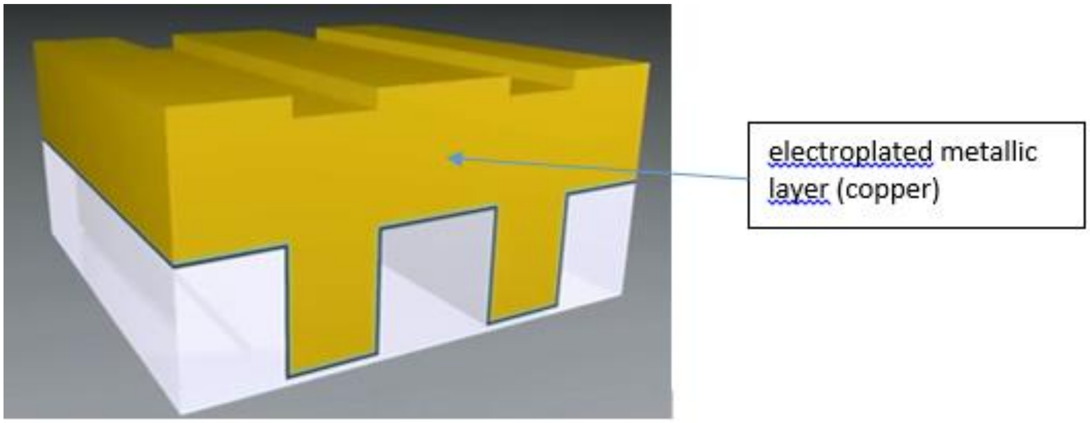




[15] *See generally* "Conformal CVD Co Deposition for Enhancement of Cu Gapfill Application," ADMETA Conference 2008, Tokyo, Japan, Exhibit 5.

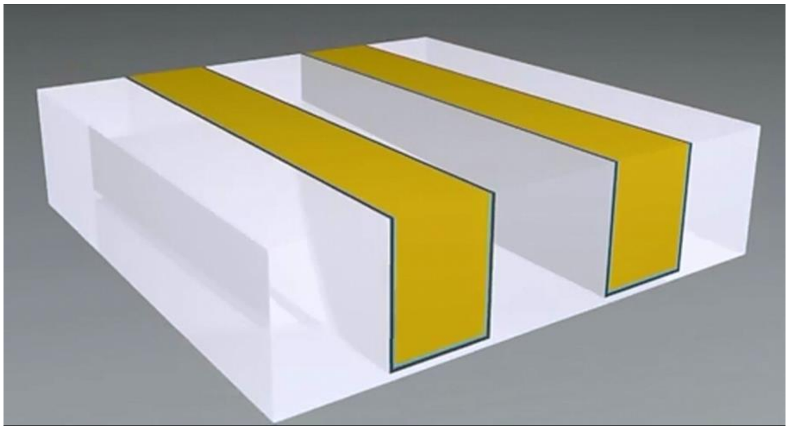
As is now well known in the art, at the geometries found in the accused chips, an optimized PVD copper seed layer at the 2x nanometer node and beyond will result in sidewall coverage at midpoint of about 13% to 15% of the thickness on the field, and certainly less than 25% of the thickness on the field.

> f. an electroplated metallic layer disposed over the second seed layer, wherein the electroplated metallic layer comprises a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals, as depicted below:



After the second substantially non-conformal seed layer is applied through a PVD process, an electroplated metallic layer of copper is disposed over the second seed layer in the openings and on the field, filling the openings.

> g. (claim 26) A metallic interconnect fabricated by using the multiple seed layer structure of claim 1, wherein the electroplated metallic layer overlying the opening and overlying the field, and the first and second seed layers overlying the field, and the barrier layer overlying the field, are substantially removed by a removal technique, said removal technique comprises one or more of a mechanical polishing technique, a chemical mechanical polishing technique, a wet etching technique, and a dry etching technique, as depicted below:



As explained in the Volta Animation, after copper is used to fill the openings and applied over the field through electroplating, the copper over the field and the barrier layer and first and second seed layers over the field are removed using a polishing technique.

COUNT II: INFRINGEMENT OF THE ’226 PATENT

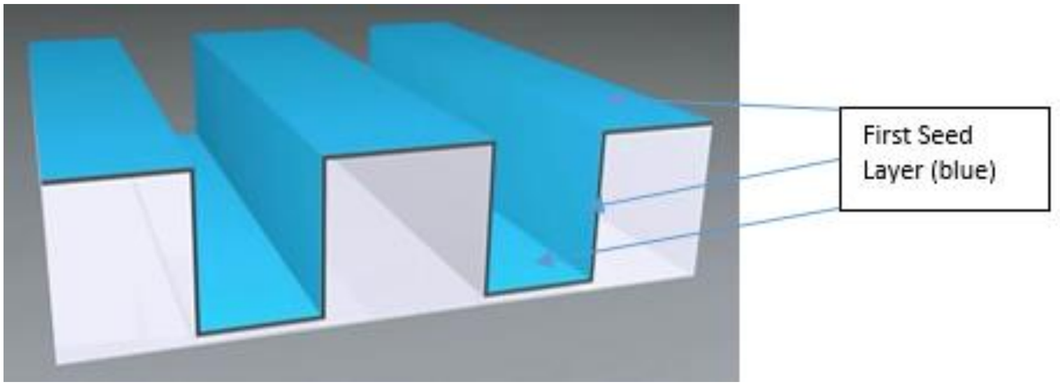
116. All preceding paragraphs are incorporated by reference as if fully set forth herein.

117. The Defendants have infringed at least one claim of the ’226 patent by performing the acts of infringement described above with respect to the Accused Chips.

118. Each of the Accused Chips is fabricated by TSMC using the same relevant fabrication method, and producing the same relevant chip structure, as explained in the Volta Animation, and as described in paragraphs 49-53 and 58-66 above. As such, the Accused Chips meet at least one claim of the ’226 patent.

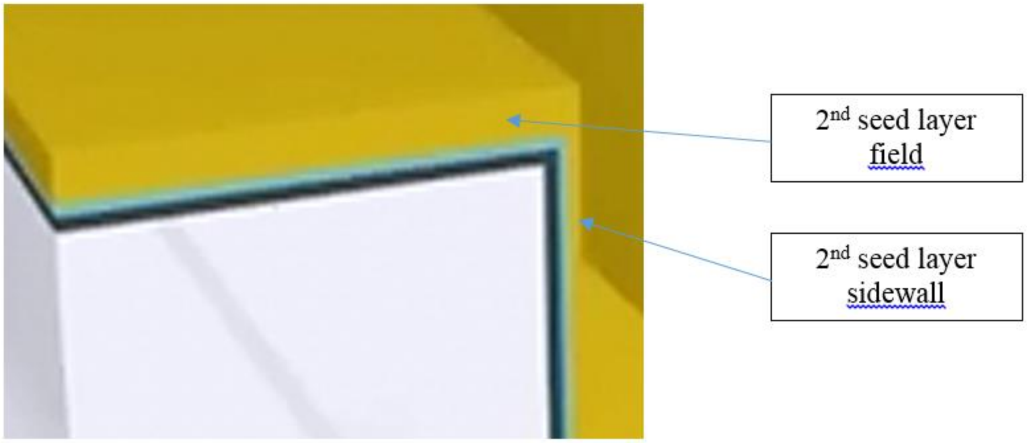
119. By way of example and not limitation, each of the Accused Chips meets or embodies every limitation of at least claim 1 of the ’226 patent in that each of the Accused Chips is fabricated using a method as recited in claim 1 by:

a. depositing a substantially conformal seed layer over the field and inside surfaces of the at least one opening;



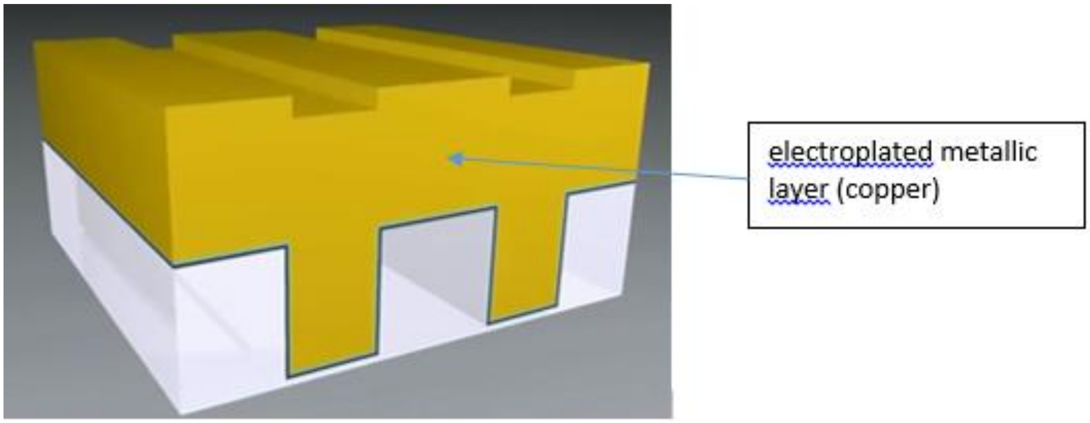
A substantially conformal layer of cobalt is deposited over the field and inside surfaces of at least one opening layer through a CVD process.

> b. depositing a substantially non-conformal seed layer over the substantially conformal seed layer, said substantially non-conformal seed layer being thicker than said substantially conformal seed layer over the field, wherein the substantially conformal and the substantially non-conformal seed layers do not seal the at least one opening; and



As depicted above and on information and belief, an optimized PVD copper seed layer at the 2x nanometer node and beyond will result in thickness over the field far greater than that of a substantially conformal CVD seed layer. Further, as depicted in the Volta Animation, the substantially conformal and the substantially non-conformal seed layers do not seal the at least one opening.

c. electroplating a metallic layer over the substantially non-conformal seed layer, wherein the electroplated metallic layer comprises a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.



After the substantially non-conformal seed layer is applied through a PVD process, an electroplated metallic layer of copper (i.e. "Cu") is disposed over the substantially non-conformal seed layer.

COUNT III: INFRINGEMENT OF THE '052 PATENT

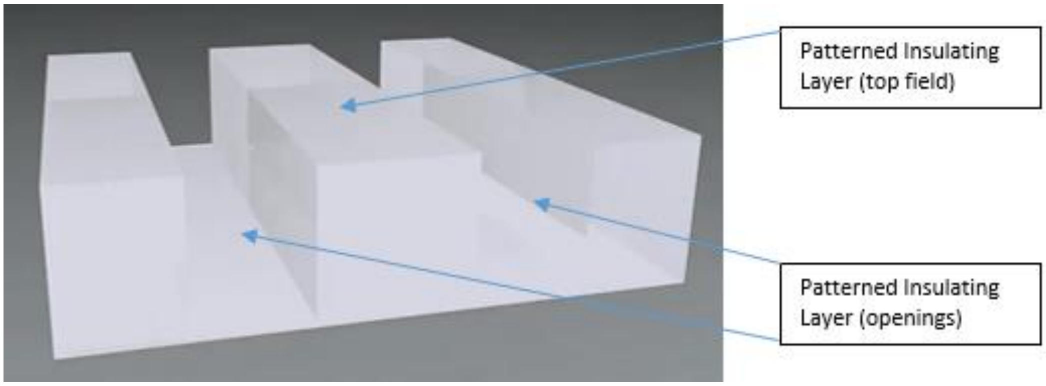
120. All preceding paragraphs are incorporated by reference as if fully set forth herein.

121. The Defendants have infringed at least one claim of the '052 patent by performing the acts of infringement described above with respect to the Accused Chips.

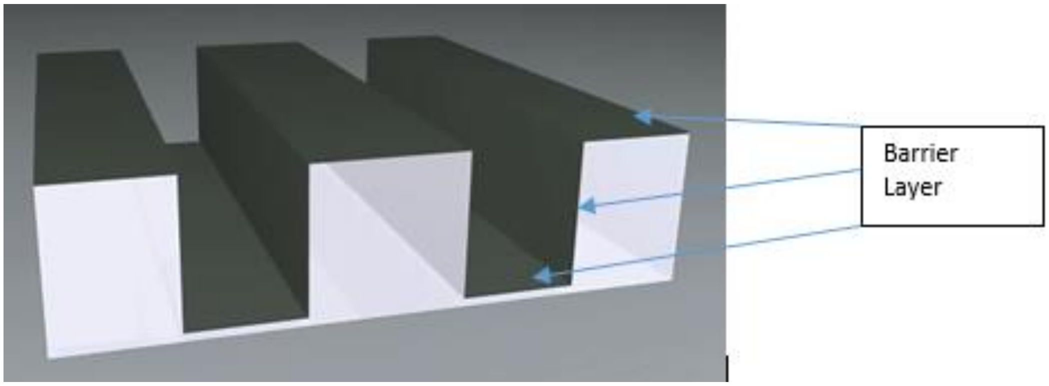
122. Each of the Accused Chips is fabricated by TSMC using the same relevant fabrication method, and producing the same relevant chip structure, as explained in the Volta Animation, and as described in paragraphs 49-53 and 58-66 above. As such, the Accused Chips meet at least one claim of the '052 patent.

123. By way of example and not limitation, each of the Accused Chips meets or embodies every limitation of at least claim 4 of the '052 patent in that each of the Accused Chips is fabricated using a method as recited in claim 4 by:

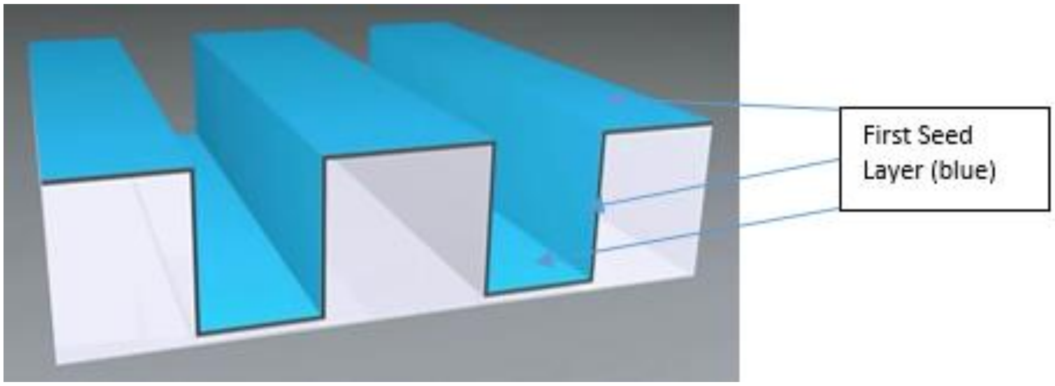
a. forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening, as depicted below;


Patterned Insulating Layer (top field)
Patterned Insulating Layer (openings)

b. depositing a barrier layer over the field and inside surfaces of the at least one opening, as depicted below;

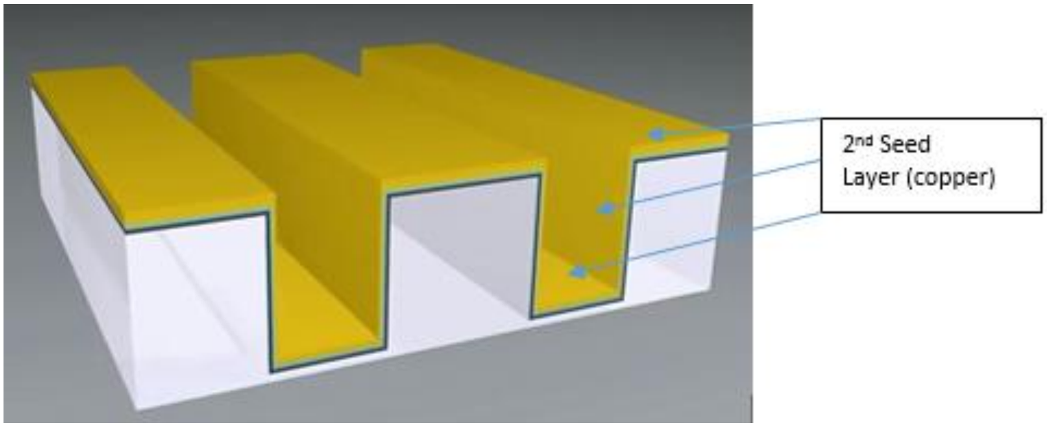

Barrier Layer

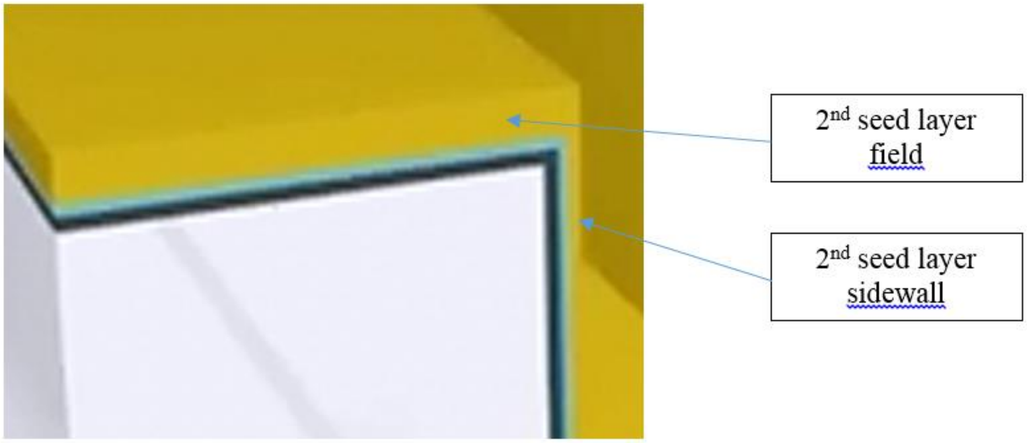
c. chemical vapor depositing a first seed layer over the barrier layer, as depicted below;


First Seed Layer (blue)

A first seed layer is deposited by a CVD technique over the barrier layer.

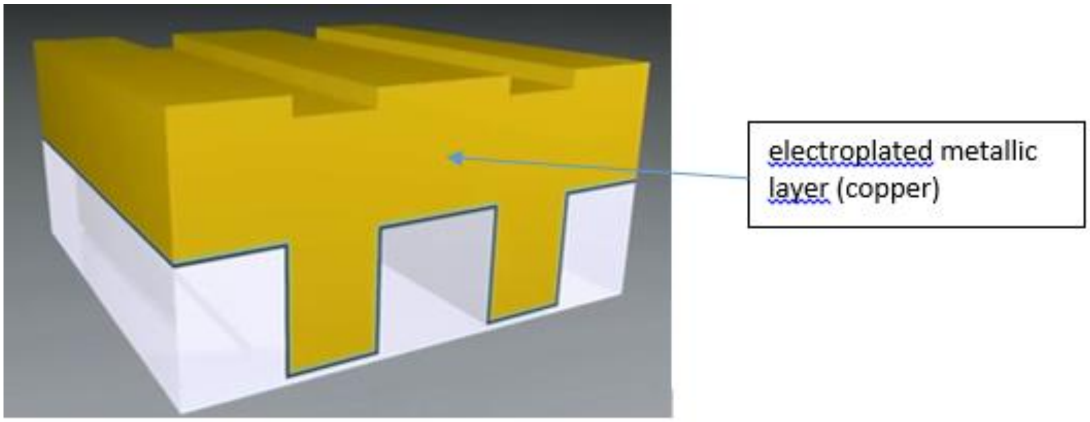
d. physical vapor depositing a second seed layer over the first seed layer, wherein the second seed layer is thicker than the first seed layer over the field, as depicted below; and


2nd Seed
Layer (copper)


2nd seed layer
field
2nd seed layer
sidewall

A second seed layer is deposited by a PVD technique over the first seed layer. The second seed layer is thicker than the first seed layer over the field.

e. filling the at least one opening by electroplating a metallic layer comprising copper or a copper alloy over the two seed layers, as depicted below.



The openings are filled by electroplating copper over the two seed layers.

COUNT IV: INFRINGEMENT OF THE ’445 PATENT

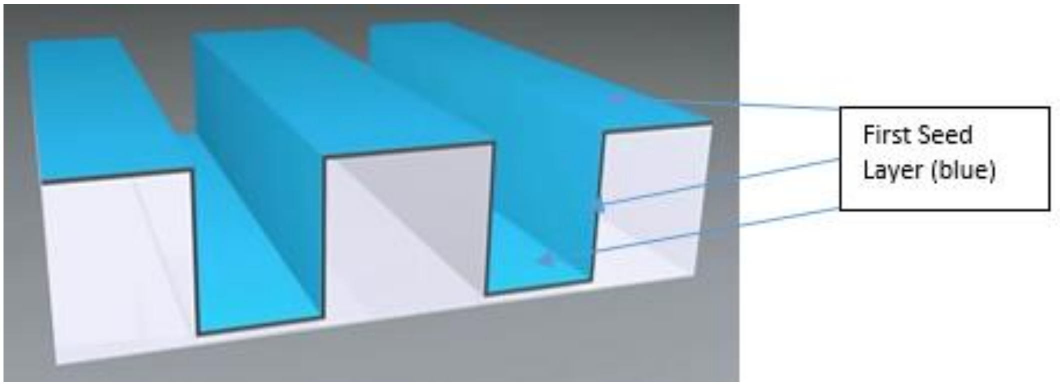
124. All preceding paragraphs are incorporated by reference as if fully set forth herein.

125. The Defendants have infringed at least one claim of the ’445 patent by performing the acts of infringement described above with respect to the Accused Chips.

126. Each of the Accused Chips is fabricated by TSMC using the same relevant fabrication method, and producing the same relevant chip structure, as explained in the Volta Animation, and as described in paragraphs 49-53 and 58-66 above. As such, the Accused Chips meet at least one claim of the ’445 patent.

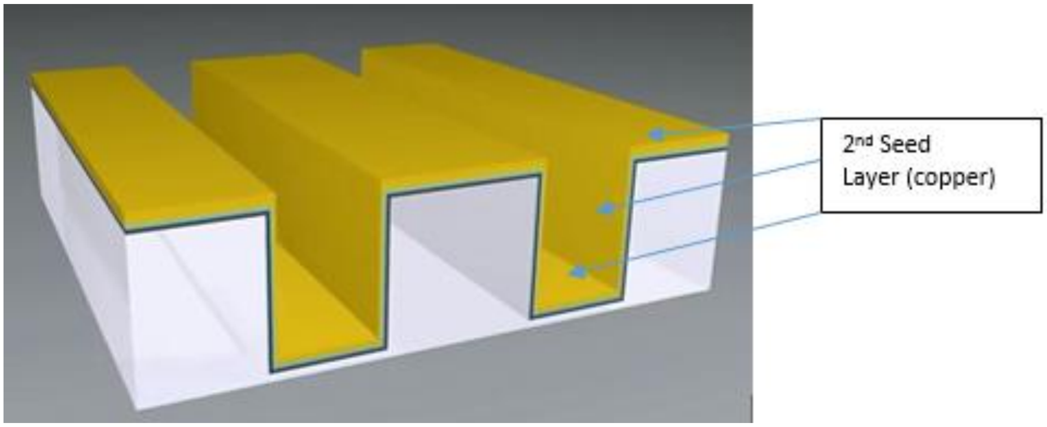
127. By way of example and not limitation, each of the Accused Chips meets or embodies every limitation of at least claim 18 of the ’445 patent in that each of the Accused Chips is fabricated using a method as recited in claim 18 by:

a. utilizing a CVD chamber capable of depositing a CVD seed layer over the sidewalls of the at least one opening;



A CVD chamber is used to deposit a first seed layer over the sidewalls of at least one opening.

b. utilizing a PVD chamber capable of depositing a PVD seed layer over the substrate;



A PVD chamber is used to deposit a second seed layer over the substrate.

c. configuring an automatic controller with recipe information, the recipe information including deposition sequence, process and timing parameters for operation of the CVD chamber and the PVD chamber;

On information and belief, use of the AMAT Volta system requires at least one automatic controller containing recipe information which includes deposition sequence, process and timing parameters for operation of the CVD chamber and the PVD chamber.

d. operating the automatic controller in accordance with the recipe information to cause the CVD chamber to deposit a CVD first seed layer over the field and the sidewalls of the at least one opening;

On information and belief, as shown in the Volta animation cited above, the said at least one automatic controller is operated in accordance with the recipe information to cause the CVD chamber to deposit a CVD first seed layer over the field and the sidewalls of the at least one opening.

> e. operating the controller in accordance with the recipe information to deposit in the PVD chamber a second seed layer over the first seed layer; and

On information and belief, as shown in the Volta animation cited above, the said at least one automatic controller is operated in accordance with the recipe information to cause the PVD chamber to deposit a second seed layer over the first seed layer and opening.

> f. operating the controller in accordance with the recipe information to stop the deposition of the first and second seed layers prior to sealing the at least one opening, thereby leaving enough room for electroplating inside the at least one opening.

On information and belief, as shown in the Volta animation cited above, the said at least one automatic controller is operated in accordance with the recipe information to stop the deposition of the first and second seed layers prior to sealing the at least one opening, thereby leaving enough room for electroplating inside the at least one opening.

DAMAGES

128. The Defendants' acts of infringement of the patents-in-suit as alleged above have injured Dr. Cohen and thus Dr. Cohen is entitled to recover damages which in no event can be less than a reasonable royalty, including his costs, and pre-judgment and post-judgment interest pursuant to 35 U.S.C. § 284.

WILLFUL INFRINGEMENT

A. Willful Infringement by TSMC

129. TSMC has infringed the ’668, ’226, ’052, and ’445 patents despite an objectively high likelihood that its actions constituted infringement of these valid patents.

130. TSMC knew or should have known this objectively high likelihood, at least because TSMC was made aware of the patents-in-suit through Dr. Cohen’s counsel.

131. On information and belief, after Dr. Cohen presented his patented technology to TSMC in person in 2001 and repeatedly reintroduced it in subsequent years (as described in paragraphs 24–34), TSMC deliberately copied or drew upon Dr. Cohen’s patented technology in developing the Accused Chips.

132. On information and belief, TSMC deliberately misrepresented its intentions to Dr. Cohen in the course of discussing his patented technology and licensing overtures, including when TSMC stated in 2006 that it “would like to leave the door open to licensing Dr. Cohen’s patents in the future, should TSMC elect to adopt multiple layer seed processes that are relevant to Dr. Cohen’s patent claims . . . .”

133. TSMC’s ongoing infringement of the patents-in-suit, copying, and misrepresentations subsequent to viewing Dr. Cohen’s in-person presentation, receiving Dr. Cohen’s multiple communications about the patents-in-suit, and declining to take a license to the patents-in-suit, constitutes egregious misconduct beyond typical infringement.

134. The infringement of the patents-in-suit alleged above has injured Dr. Cohen and thus, Dr. Cohen is entitled to recover damages adequate to compensate for TSMC’s infringement, which in no event can be less than a reasonable royalty.

135. Because TSMC willfully infringed the patents-in-suit, Dr. Cohen is permitted under 35 U.S.C. § 284 to recover treble the amount of actual damages sustained by the Plaintiff.

EXCEPTIONAL CASE

136. TSMC's acts, including at least their willful infringement, have made the present case exceptional pursuant to 35 U.S.C. § 285 and/or other applicable authority. Therefore, Dr. Cohen is entitled to attorneys' fees as the prevailing party.

DEMAND FOR JURY TRIAL

137. Dr. Cohen hereby demands a jury trial on all claims and issues triable of right by a jury.

PRAYER

WHEREFORE, Dr. Cohen prays for entry of judgment in his favor against each and every defendant:

A. Finding that Taiwan Semiconductor Manufacturing Company, Ltd. has infringed one or more claims of the '668 patent, one or more claims of the '226 patent, one or more claims of the '052 patent, and one or more claims of the '445 patent;

B. Finding that TSMC North America Corp. has infringed one or more claims of the '668 patent, one or more claims of the '226 patent, one or more claims of the '052 patent, and one or more claims of the '445 patent;

C. Finding that Huawei Technologies Co., Ltd. has infringed one or more claims of the '668 patent, one or more claims of the '226 patent, one or more claims of the '052 patent, and one or more claims of the '445 patent;

D. Finding that Huawei Device USA Inc. has infringed one or more claims of the '668 patent, one or more claims of the '226 patent, one or more claims of the '052 patent, and one or more claims of the '445 patent;

E. Finding that Futurewei Technologies, Inc. has infringed one or more claims of the ‘668 patent, one or more claims of the ’226 patent, one or more claims of the ’052 patent, and one or more claims of the ’445 patent;

F. Finding that HiSilicon Technologies Co., Ltd. has infringed one or more claims of the ‘668 patent, one or more claims of the ’226 patent, one or more claims of the ’052 patent, and one or more claims of the ’445 patent;

G. Finding that Apple, Inc. has infringed one or more claims of the ‘668 patent, one or more claims of the ’226 patent, one or more claims of the ’052 patent, and one or more claims of the ’445 patent;

H. Awarding Dr. Cohen all allowable damages flowing from the defendants’ infringement of the ‘668 patent, the ’226 patent, the ’052 patent, and the ’445 patent, which can be no less than a reasonable royalty under 35 U.S.C. § 284;

I. Finding that Taiwan Semiconductor Manufacturing Company, Ltd. and TSMC North America Corp. have willfully infringed the ‘668 patent, the ’226 patent, the ’052 patent, and the ’445 patent, and awarding Dr. Cohen all allowable damages for their willful infringement, including but not limited to an award of three times Dr. Cohen’s actual damages pursuant to 35 U.S.C. § 284;

J. Awarding Dr. Cohen his costs, and pre-judgment and post-judgment interest on his damages caused by the defendants’ infringement of the ‘668 patent, the ’226 patent, the ’052 patent, and the ’445 patent, and/or otherwise, as the Court may deem just;

K. Declaring this case exceptional, in Dr. Cohen’s favor, and awarding Dr. Cohen his attorneys’ fees in this action pursuant to 35 U.S.C. § 285 and/or other applicable authority; and

L. Granting Dr. Cohen such other and further legal and/or equitable relief that is just and proper under the circumstances.

Dated: May 5, 2017

Respectfully submitted,

/s/ Christopher M. Faucett
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